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7. (Amended) The method of claim ~~6~~, further comprising the steps of:

h) forming an upper-level dielectric film on the interlevel dielectric film after the e) has been performed;

Cont'd

i) forming two contact holes which pass through the upper-level dielectric film to reach the intermediate and control gate electrodes of the ferroelectric FET, respectively, and then filling the contact holes with a conductor material to form first and second contact members, which make electrical contact with the intermediate and control gate electrodes, respectively; and

j) forming first and second interconnects, which are connected to the first and second contact members, respectively, on the upper-level dielectric film.

REMARKS

The Examiner's non-final Office Action dated April 1, 2002 has been received and its contents carefully noted. Applicant respectfully submits that this response is timely filed and fully responsive to the Office Action.

Claims 1-7 were pending in the present application, of which claims 1 and 6 are independent. By this amendment, claim 5 is canceled and claims 1 and 6 are amended. Applicant respectfully contends that no issue of new matter is presented by the aforementioned amendment. Accordingly, claims 1-7 remain pending, and are believed to be in condition for allowance for at least the following reasons.

A. 35 U.S.C. §112, 2nd Paragraph Rejection

Claims 1-7 stand rejected under 35 U.S.C. § 112, second paragraph as indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In particular, the Examiner inquires as to the location of the ferroelectric film formed relative to the other elements of the ferroelectric FET. By the above actions, claim 1 is amended so as to recite that the ferroelectric film is formed over the semiconductor substrate. Claim 6 requires no further amending in this regard since it already recites that the ferroelectric film "is in contact with an upper surface of the intermediate electrode and that the control gate

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electrode faces the intermediate electrode with the ferroelectric film interposed therebetween." Reconsideration and withdrawal of the rejection is respectfully requested.

B. 35 U.S.C. §102 Rejection

Claims 1-6 stand rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 4,888,630 to Paterson. By the above actions, claim 5 is canceled, however, the subject matter recited therein is incorporated into independent claims 1 and 6. It is respectfully contended that the claimed invention as presently amended clearly defines over Paterson for at least the reasons that follow.

In accordance with claims 1-4, the claimed invention is directed to a semiconductor device comprising an MISFET provided on a semiconductor substrate, a ferroelectric FET provided on the semiconductor substrate, a memory circuit block, in which the ferroelectric FET are arranged, and a control circuit block, in which the MISFET is arranged, for controlling the memory circuit block.

In accordance with claims 6 and 7, the claimed invention is directed to a method for fabricating a semiconductor device comprising the steps of forming a gate insulating film and a gate electrode for each of first- and second-channel-type MISFETs and a ferroelectric FET over a semiconductor substrate, forming a memory circuit block, in which the ferroelectric FET is arranged, and forming a control circuit block, in which the MISFET is arranged, for controlling the memory circuit block.

Paterson Fails to Teach the Claimed Invention

It is respectfully contended that Paterson fails to expressly teach or inherently suggest each and every claim feature necessary to anticipate the claimed invention under 35 U.S.C. §102. For instance, the Examiner indicates that Paterson teaches a semiconductor device that allegedly reads on the claimed invention.

However, in accordance with the claimed invention as presently amended, the semiconductor device requires the combination of:

(1) a memory circuit block (in which ferroelectric FETs are arranged), and

(2) a control circuit block (in which MISFETs are arranged) for controlling the memory circuit block, the memory circuit block and the control circuit block being provided on the same substrate. This is advantageous since it allows the formation of a large-scale integrated circuit having logic circuit including a memory device and an operating circuit integrated thereon, such as system LSI.

On the other hand, Paterson teaches a memory cell where a ferroelectric FET and an MISFET are formed on the same substrate, and a path transistor (14), which corresponds to the MISFET. The path transistor (14), however, corresponds to the selective transistor of claim 6 of the present invention, which is used for selecting ferroelectric memory cell and is provided in the memory circuit block. Hence, in contrast to the claimed invention, the path transistor (14) of Paterson is not provided in the control circuit block.

Therefore, the object of the invention of Paterson is different from that of the claimed invention, which is to obtain a highly integrated semiconductor device that includes a memory array with a ferroelectric FET provided thereon as a memory cell, and a logic circuit such as processor and the like. Consequently, the teachings of Paterson cannot achieve the effect of the claimed invention, in particular, obtaining an integrated semiconductor device whereby a memory and a transistor for controlling the memory are integrated on the same substrate.

C. 35 U.S.C. §103 Rejection

Claim 7 stands rejected under 35 U.S.C. §103(a) as unpatentable over Paterson. Insofar as Paterson clearly fails to expressly teach or implicitly suggest each and every feature set forth in base claim 6, it is respectfully contended that claim 7 cannot be rendered *prima facie* obvious since it incorporates by reference the features of claim 6. In particular, in addition to requiring additional method steps, claim 7 also requires the steps of forming a memory circuit block in which the ferroelectric FET is arranged, and forming a control circuit block in which the MISFET is arranged, for controlling the memory circuit block. As previously mentioned in response to the §102 rejection, Paterson fails to teach, disclose or suggest such features. Accordingly, reconsideration and withdrawal of the rejection is earnestly solicited.

Conclusion

Having responded to all rejections set forth in the outstanding non-final Office Action, it is submitted that the claims are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

Donald R. Studebaker
Registration No. 32,815

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

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MARKED-UP VERSION OF THE AMENDED CLAIMS

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an MISFET, which is provided on the semiconductor substrate and includes a gate insulating film, a gate electrode and source/drain regions; [and]

a ferroelectric FET, which is provided on the semiconductor substrate and includes a ferroelectric film provided over the semiconductor substrate, a control gate electrode provided on the ferroelectric film and source/drain regions;

a memory circuit block, in which the ferroelectric FET is arranged; and

a control circuit block, in which the MISFET is arranged, for controlling the memory circuit block.

6. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

a) forming a gate insulating film and a gate electrode for each of first- and second-channel-type MISFETs and a ferroelectric FET over a semiconductor substrate;

b) implanting ions of a dopant for forming source/drain regions from over the gate electrode of the ferroelectric FET and the gate electrode of one of the first- and second-channel-type MISFETs;

c) implanting ions of another dopant for forming source/drain regions from over the gate electrode of the other MISFET;

d) forming an interlevel dielectric film covering the gate electrodes of the MISFETs and the ferroelectric FET, forming a contact hole, which passes through the interlevel dielectric to reach the gate electrode of the ferroelectric FET, and then filling the contact hole with a conductor material to form a contact member; [and]

e) forming an intermediate electrode, a ferroelectric film and a control gate electrode over the interlevel dielectric film so that the intermediate electrode is connected to the contact member and that the ferroelectric film is in contact with an upper surface of the intermediate

electrode and that the control gate electrode faces the intermediate electrode with the ferroelectric film interposed therebetween;

f) forming a memory circuit block, in which the ferroelectric FET is arranged; and

g) forming a control circuit block, in which the MISFET is arranged, for controlling the memory circuit block.

7. (Amended) The method of claim 6, further comprising the steps of:

[f)] h) forming an upper-level dielectric film on the interlevel dielectric film after the step e) has been performed;

[g)] i) forming two contact holes which pass through the upper-level dielectric film to reach the intermediate and control gate electrodes of the ferroelectric FET, respectively, and then filling the contact holes with a conductor material to form first and second contact members, which make electrical contact with the intermediate and control gate electrodes, respectively; and

[h)] j) forming first and second interconnects, which are connected to the first and second contact members, respectively, on the upper-level dielectric film.